CLAIMS

1. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

a first controller that controls access to the plurality of memory locations by a first device; and

a second controller that operates independently of the first controller and controls access to the plurality of memory locations by a second device.

2. The system of claim 1, wherein the second controller comprises a data transfer engine that transfers data from a lower-level memory to the memory locations.

3. The system of claim 2, wherein the data transfer engine transfers data from the memory locations to the lower-level memory.

4. The system of claim 3, wherein the data transfer engine comprises a DMA controller.

5. The system of claim 2, wherein the data transfer engine comprises a DMA controller.

6. The system of claim 1, wherein the second controller comprises a DMA controller which provides at least one first address identifying at least one memory location of the second device from which data sets are to be transferred, and at least one second address identifying at least one memory location of the cache to which the data sets are to be transferred.

7. The system of claim 6, wherein the DMA controller is configured such that the second address can be incremented or decremented between consecutively transferred data sets without also incrementing or decrementing the first address between the consecutively transferred data sets.

8. The system of claim 6, wherein the DMA controller is configured such that the second address can be incremented or decremented between consecutively transferred data

sets by a different amount than the first address is incremented or decremented between the consecutively transferred data sets.

9. The system of claim 1, wherein the first and second controllers are integrated on a common semiconductor die.

10. The system of claim 1, wherein each of the plurality of memory locations has only a single word line associated therewith.

11. The system of claim 1, further comprising:

an address input for selecting memory locations to be accessed; and

at least one first multiplexer that selects addresses to be provided to the address input from among addresses provided by the first device and addresses provided by the second controller.

12. The system of claim 11, further comprising at least one second multiplexer that selects an external address to be provided to the second device from among external addresses provided by the first device and external addresses provided by the second controller.

13. The system of claim 11, further comprising:

an address output for outputting addresses retrieved from memory locations along with data associated therewith; and

at least one second multiplexer that selects external addresses to be provided to the second device from among the addresses provided at the address output and external addresses provided by the second controller.

14. The system of claim 1, further comprising a third controller that controls arbitration for shared cache resources among the first controller and the second controller.

15. The system of claim 1, in combination with the first device, wherein the first device comprises a processor.

16. The combination of claim 15, wherein the processor comprises a digital signal processor.

17. The system of claim 5, in combination with the first device, wherein the first device comprises a digital signal processor.

18. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

an address input that receives addresses from either one of a first device and a second device, the addresses provided on the address input identifying memory locations to be accessed; and

at least one first multiplexer that selects addresses to be provided to the address input from among addresses provided by the first device and addresses provided by the second device.

19. The cache memory system of claim 18, further comprising a line-fill buffer configured and arranged to transfer lines of data and addresses associated with the lines data into the plurality of memory locations, wherein an output of the at least one first multiplexer is coupled to an address input of the line-fill buffer.

20. The system of claim 18, further comprising at least one second multiplexer that selects an external address to be provided to a third device from among external addresses provided by the first device and external addresses provided by the second device.

21. The system of claim 18, further comprising:

an address output for outputting addresses retrieved from memory locations along with data associated therewith; and

at least one second multiplexer that selects external addresses to be provided to the third device from among the addresses provided at the address output and external addresses provided by the second device.

22. The system of claim 18, in combination with the first device, wherein the first device comprises a processor.

23. The combination of claim 22, further in combination with the second device, wherein the second device comprises a data transfer engine.

24. The combination of claim 23, wherein the data transfer engine comprises a DMA controller.

25. The system of claim 18, in combination with the second device, wherein the second device comprises a data transfer engine.

26. The combination of claim 25, wherein the data transfer engine comprises a DMA controller.

27. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

an address output for outputting addresses retrieved from memory locations along with data associated therewith; and

at least one multiplexer that selects external addresses to be provided to a first device from among the addresses provided at the address output and external addresses provided by a second device.

28. The cache memory system of claim 27, further comprising a copy-back buffer configured and arranged to transfer lines of data and addresses associated with the lines of data out of the plurality of memory locations, wherein an output of the at least one multiplexer is coupled to an address input of the copy-back buffer.

29. The system of claim 28, in combination with the second device, wherein the second device comprises a data transfer engine.

30. The combination of claim 29, wherein the data transfer engine comprises a DMA controller.

31. The combination of claim 30, further in combination with the first device, wherein the first device comprises a lower-level memory.

32. The system of claim 29, in combination with the first device, wherein the first device comprises a lower-level memory.

33. A method, comprising an act of:

(a) accessing memory locations of an associative cache independently of a cache controller that controls access to memory locations of the cache by a processor.

34. The method of claim 33, wherein the act (a) includes using a data transfer engine to transfer data from a lower-level memory to the memory locations of the cache.

35. The method of claim 34, wherein the act (a) includes using the data transfer engine to transfer data from the memory locations of the cache to the lower-level memory.

36. The method of claim 33, wherein each of the memory locations has only a single word line associated therewith.

37. The method of claim 33, wherein the act (a) includes using a DMA controller to transfer data from a lower-level memory to memory locations of the cache, the DMA controller providing at least one first address identifying at least one memory location of the lower-level memory from which data sets are to be transferred, and further providing at least one second address identifying at least one of the plurality of memory locations to which the data sets are to be transferred.

38. The method of claim 37, wherein the act (a) further includes incrementing or decrementing the second address between consecutively transferred data sets without also incrementing or decrementing the first address between the consecutively transferred data sets.

39. The method of claim 37, wherein the act (a) further includes incrementing or decrementing the second address between consecutively transferred data sets by a different

amount than the first address is incremented or decremented between the consecutively transferred data sets.

40. A method, comprising acts of:

selecting addresses to be provided to an address input of an associative cache from among addresses provided by a first device and addresses provided by a second device; and

accessing memory locations within the cache based upon the selected addresses provided to the address input of the cache.

41. The method of claim 40, further comprising an act of:

selecting external addresses to be provided to a third device from among external addresses provided by the first device and external addresses provided by the second device.

42. The method of claim 40, further comprising acts of:

outputting addresses retrieved from memory locations of the cache along with data associated therewith; and

selecting external addresses to be provided to a third device from among the addresses output from the cache and external addresses provided by the second device.

43. The method of claim 40, wherein each of the memory locations has only a single word line associated therewith.

44. The method of claim 40, further comprising an act of:

providing the selected addresses to a line-fill buffer which then provides the selected addresses to the address input of the associative cache.

45. A method, comprising acts of:

outputting addresses retrieved from memory locations of a cache along with data associated therewith; and

selecting external addresses to be provided to a first device from among the addresses output from the cache and external addresses provided by a second device.

46. The method of claim 45, further comprising an act of:

providing the selected external addresses to a copy-back buffer which then provides the selected external addresses to the first device.

47. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data; and

means for accessing memory locations of the cache independently of a cache controller that controls access to memory locations of the cache by a processor.

48. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

an address input that receives addresses from either one of a first device and a second device, the addresses provided on the address input identifying memory locations to be accessed; and

means for selecting addresses to be provided to the address input from among addresses provided by the first device and addresses provided by the second device.

49. The system of claim 48, further comprising means for accessing memory locations based upon the selected addresses provided to the address input.

50. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

an address output for outputting addresses retrieved from memory locations along with data associated therewith; and

means for selecting external addresses to be provided to a first device from among the addresses output from the cache and external addresses provided by a second device.

51. A cache memory system, comprising:

a data array including memory locations for storing data;

a tag array including memory locations for storing tags associated with the data stored in the data array;

a first controller that controls access to the tag and data arrays by a first device;

a second controller that controls access to the tag and data arrays by a second device; and

a third controller that controls arbitration for cache resources shared by the first and second controllers.

52. The system of claim 51, wherein the first and second controllers are configured and arranged to access the tag and data arrays independently of one another.

53. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data; and

a controller that controls access to the plurality of memory locations by a device, the controller being configured to provide at least one first address identifying at least one memory location of the device from which data sets are to be transferred, and at least one second address identifying at least one memory location of the cache to which the data sets are to be transferred, the controller being further configured such that the second address can be incremented or decremented between consecutively transferred data sets without also incrementing or decrementing the first address between the consecutively transferred data sets.

54. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data; and

a controller that controls access to the plurality of memory locations by a device, the controller being configured to provide at least one first address identifying at least one memory location of the device from which data sets are to be transferred, and at least one second address identifying at least one memory location of the cache to which the data sets are to be transferred, the controller being further configured such that the second address can be incremented or decremented between consecutively transferred data sets by a different amount than the first address is incremented or decremented between the consecutively transferred data sets.

55. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

means for controlling access to the plurality of memory locations by a device;

means for providing at least one first address identifying at least one memory location of the device from which data sets are to be transferred, and at least one second address identifying at least one memory location of the cache to which the data sets are to be transferred; and

means for incrementing or decrementing the second address between consecutively transferred data sets without also incrementing or decrementing the first address between the consecutively transferred data sets.

56. A cache memory system, comprising:

a plurality of memory locations to store data and addresses associated with the data;

means for controlling access to the plurality of memory locations by a device;

means for providing at least one first address identifying at least one memory location of the device from which data sets are to be transferred, and at least one second address identifying at least one memory location of the cache to which the data sets are to be transferred; and

means for incrementing or decrementing the second address between consecutively transferred data sets by a different amount than the first address is incremented or decremented between the consecutively transferred data sets.